Remarks

Claims 1and 3-13 are pending in this application. Claims 1 and 13 have been amended, and claim 2 has been canceled. The Examiner has rejected claims 1, 2 and 5-13 and has objected to claims 3 and 4 as depending from rejecting claims. The Examiner has rejected claims 1, 2, 5, 6, 9 and 11-13 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,794, 729 to Mori et al. The Examiner has also rejected claims 7, 8, and 10 under 35 U.S.C. §103(a) as being obvious in light of Mori et al.

The Examiner has declared claims 3 and 4 to be allowable if rewritten in independent form so as not to depend from a rejected base claim and to include all of the limitations of the rejected base claim and any intervening claims.

In view of the amendments and remarks herein, the undersigned respectfully requests reconsideration of these rejections and submits that the application is now in condition for allowance.

Rejection of Claims 1, 2, 5, 6 ,9, and 11-13 under 35 U.S.C. § 102(e)

The Examiner has rejected claims 1, 2, 5, 6, 9, and 11-13 under 35 U.S.C. § 102(e) as being anticipated by Mori et al. Respectfully, the Applicant strongly disagrees with the Examiner's assertion that Mori et al. anticipates the present invention. The Applicant does not believe that Mori et al. discloses an electrical component structure comprising a plurality of overlying substantially parallel layers, where each layer is a lattice formed from orthogonally arranged and electrically connected conductive tracks, provided with conductive islands in the windows of the lattice, which are electrically connected to intersect regions of the lattice of an

adjacent layer, as claimed in independent claims 1, 12, and 13. The Applicant's reasons for disagreeing with the Examiner on this point become apparent by consideration of the drawings presented below.

Figure 1 below is a drawing prepared by Applicant of the stacked capacitor of Mori et al. It combines Figures 2A, 2B and 2C of Mori et al. into a single drawing. More particularly, the upper surface of the capacitor 8 shown in the drawing corresponds to Figure 2A, the front surface corresponds to Figure 2B, and the right hand surface corresponds to Figure 2C. Note that the drawing actually shows the capacitor in an upside down position, as the electrodes formed on the surface shown in Figure 2A of Mori et al. are on the bottom surface of the capacitor. Therefore, when comparing the front and right side representations of the capacitor with Figures 2B and 2C, bear in mind that it will be necessary to consider Figure 2B and 2C upside down.

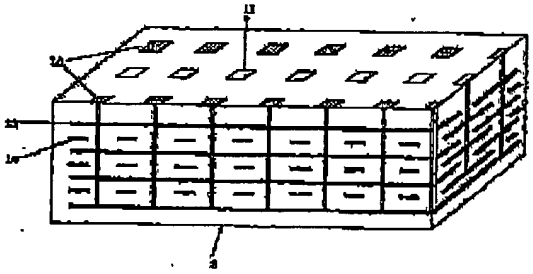


Figure 1 - US 6,794,729 Figs 2A-2C combined

With reference to the enclosed Figure 1 and Figures 2A, 2B and 2C of Mori et al., it will be seen that the capacitor of Mori et al. comprises a plurality of electrode layers 13 and 14, connected by vertical vias to electrodes 10 and 11 formed on the bottom surface of the capacitor.

In the cross section of Figure 2B (i.e. the front wall of our drawing) the layer 13 is shown as a continuous layer, whereas the layer 14 is shown as a broken layer between the vertical vias. In contrast, in Figure 2C (the right hand wall of our drawing) both layers 13 and 14 are broken about the vertical vias extending from the electrodes. It should be noted that the cross sections of Figures 2B and 2C are taken through the electrodes and hence the vertical vias extending vertically therefrom.

The Applicant has considered the Examiner's comments set out in the final Office Action and is still of the opinion that Mori et al. does not definitively disclose overlaid lattice structures provided with vias electrically connecting the lattice layers as specified in the original claims in this application. Although the Applicant appreciates the Examiner's detailed arguments, the Applicant respectfully submits that the Examiner may be assuming information that is not in fact shown in any of Figures 2A, 2B or 2C of Mori et al. In particular, while Figures 2B and 2C appear to show that the layer 14 may be a lattice arrangement, as explained by the Examiner, the Applicant disagrees that the same holds true for layer 13, as nowhere in either Figure 2B or 2C is it actually shown that the layer forms windows around the vias leading from electrodes 11. Instead, layer 13 could just form strips of metal extending underneath the electrodes 10, or some other arrangement. It is, therefore, in the Applicant's view simply not clear that the layer 13 comprises a lattice structure as originally claimed by Applicant, with a first set of conductive tracks arranged substantially orthogonal to and electrically connected with a second set of conductive tracks.

However, even if Applicant were to accept the Examiner's arguments about the structure of layers 13 and 14, Applicant nonetheless disagrees that independent claim 1, as amended herein to

incorporate the limitations of canceled dependent claim 2, and independent claim 12 are anticipated by Mori et al., as these claims claim that "intersect regions of the sets of tracks of the lattice of one layer are electrically connected to the conductive islands of an adjacent layer," or alternatively that "the lattice intersect points of the layers being electrically connected to the conductive islands of an adjacent layer." Similarly, claim 13 as amended herein is also not anticipated by Mori et al., as it recites "electrically connecting intersect regions of the sets of tracks of the lattice of one layer to the conductive islands of an adjacent layer." The common feature is that intersect points of the tracks of one layer are connected to islands located in the windows of the lattice of the adjacent layer. This feature presents advantages as described at page 8, lines 20-24 of the application because "current in any conductive element will flow substantially at right angles with respect to current flow in any adjacent conductive element not connected to the same capacitor terminal. Accordingly, there is minimal electromagnetic interaction between the conductive elements of the different groups, and inductive parasitic effects are reduced." This feature of having the intersect points of one layer connected to the conductive islands of an adjacent layer cannot be present on the Examiner's interpretation of Mori et al.

To explain this point further, one must consider the arrangement of electrodes as shown in Figure 2A of Mori et al. Here, it will be seen that the electrodes 10 and 11 are arranged in both horizontal and vertical rows. That is, each alternating row 10 or 11 of electrodes is not diagonally offset from each other. Turning to the Examiner's explanation of the structure of the layers 13 and 14, the significance of this will become apparent. According to the Examiner, layer 14 comprises tracks running, with reference to Figure 2A of Mori et al., from left to right underneath electrodes 11,

and tracks running from top to bottom between electrodes 10 (and presumably also electrodes 11, as they are in line). The Examiner also says that the same holds true for layer 13 except that the left to right tracks extend under the electrodes 10, the assumption being that the orthogonal tracks run between the electrodes from top to bottom of Figure 2A. Thus, layer 13 would form windows around the vias extending from the electrodes 11, and layer 14 would form windows around the vias extending from the electrodes 10.

The important point with such a structure is that the intersects between the orthogonal sets of tracks in any one layer occur in the regions between the electrodes. However, the vias extending from the electrodes extend perpendicularly downwards. Therefore, the vias extending from the respective electrodes cannot attach to the intersect regions of the assumed lattice of layers 13 and 14, but must instead connect with track portions running between the intersect regions. This arises by one of the layers being offset from the other layer only in one direction, thereby allowing the electrodes to be aligned, and not in two directions so as to give a diagonal offset as in claimed embodiments of the present invention.

Enclosed Figures 2 and 3 represent the possible Mori et al. structure as alleged by the Examiner with the respective lattice layers offset only in one direction. As shown in Figure 2, the vias extending from the windows in layer 14 intersect the tracks of layer 13 in middle areas other than intersect portions. Likewise, the vias extending upwards from the windows of layer 13 intersect with the middle of the tracks of layer 14, rather than the intersect regions.

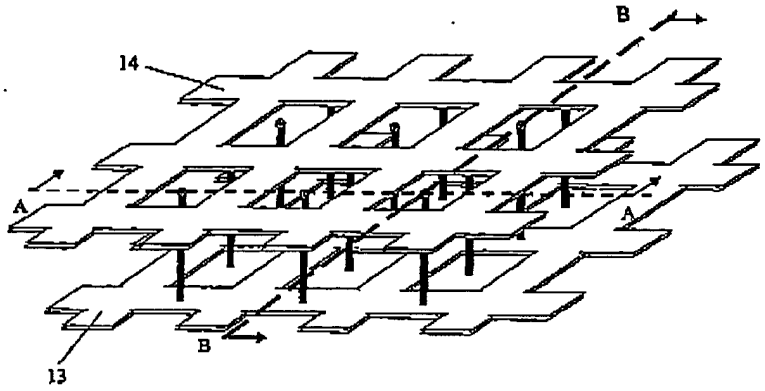


Figure 2 – Representation of Possible Mori et al. Structure as Alleged by Examiner

The cross-sections are shown in Figure 3; comparison of the cross-section along line A-A, shown as the upper drawing in Figure 3, with Figure 2B of Mori et al. and comparison of the cross-section along line B-B, shown as the lower drawing in Figure 3, with Figure 2C of Mori et al. shows that the structures are essentially the same.

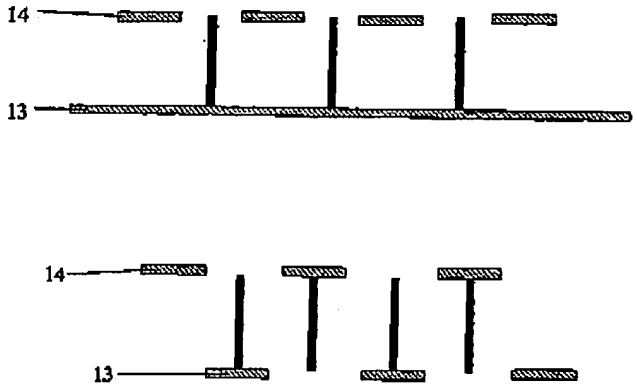


Figure 3 – Cross sections of Figure 2 – Upper drawing shows cross section along A-A in Figure 2; lower drawing shows cross section along B-B

Please note that the exact layer arrangement of Mori et al. cannot be definitively determined, as no view is shown of any of the actual layers other than the orthogonal cross sections. Given the orthogonal cross sections present in Figures 2B and 2C there could be several different layer arrangements which would present such cross sections. However, a lattice arrangement in which the conductive islands of one layer are electrically connected to intersect regions of an adjacent layer as claimed in the present invention would not present such cross sections, as discussed above. For these reasons, the Applicant respectfully requests that the Examiner withdraw the rejections.

Rejection of claims 7, 8, and 10 under 35 U.S.C. 103(a)

The Examiner has rejected claims 7, 8, and 10 under 35 U.S.C. § 103(a) as being obvious in light of Mori et al. as applied to claims 1, 2, 5, 6, 9, and 11-13. Claims 7, 8, and 10 depend either directly or indirectly from claim 1. Because, as discussed above, Mori et al. does not teach the underlying base claim, the Applicant sincerely believes that the rejections cannot stand and respectfully requests the Examiner to withdraw them.

Allowable Subject Matter

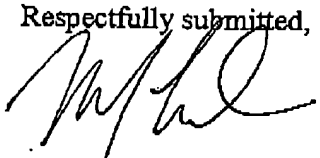
The Examiner has objected to claims 3 and 4 as depending from a rejected base claim and further stated that they would be allowable if appropriately amended in independent form. The Applicant thanks the Examiner for finding these claims allowable. However, as stated above, the Applicant sincerely believes that the underlying base claim is in form for allowance and therefore has not amended claims 3 and 4.

Conclusion

If the Examiner believes that there are any issues that can be resolved by a telephone conference, or that there are any informalities that can be corrected by an amendment, please phone the undersigned at 404-815-6061.

Applicant believes that no fees are due for this amendment. However, the Commissioner is hereby authorized to charge any deficiencies or credit any overpayment to Deposit Account No. 11-0855.

Respectfully submitted,



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